News Release

SmartDV™

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SmartDV Supports RISC-V Movement with TileLink Verification IP for RISC-V Based Systems

First Verification IP Solutions Provider with Smart TileLink VIP Model

SAN JOSE, CALIF — February 6, 2019 — SmartDV™ Technologies, the ***Proven*** and ***Trusted*** choice for Verification IP, today introduced TileLink VIP to verify the TileLink chip-scale interconnect standard, an open-source, high-performance and scalable cache-coherent fabric for RISC-V based system on chip (SoC) designs.

In making the announcement, SmartDV becomes the first VIP solutions provider to offer a smart way to verify the TileLink fabric and reduce verification time. According to Deepak Kumar Tala, chairman of SmartDV, “60-80% of a project’s resources are spent on verification to ensure design success. Given the enthusiasm for RISC-V and TileLink’s importance within the open source RISC-V ISA, investing in a VIP solution for TileLink was an easy decision.”

SmartDV's TileLink VIP helps speed the implementation and comprehensive verification of TileLink as the interconnect fabric for RISC-V or alternative architecture SoC projects. It is fully compliant with standard TileLink specifications and offers faster testbench development, more complete verification with built- in coverage analysis and simplified results analysis. An easy-to-use command interface simplifies testbench control and master/slave configurations. TileLink VIP runs on the most popular simulation environments, such as Synopsys VCS®, Cadence's Incisive® Enterprise Simulator and ModelSim ® and Questa® from Mentor, a Siemens Business.

Features include support for TileLink uncached lightweight and heavy weight and TileLink cached conformance levels, as well as cache-coherent shared memory and FIFO memory and constrained randomization of protocol attributes. It has the ability to inject errors during data transfer and configure the width of all signals. A rich set of configuration parameters control TileLink functionality. With on-the-fly protocol and data checking, it notifies the testbench of significant events — transactions, warnings, timing and protocol violations, for example.

TileLink VIP comes with a complete test suite to test every feature of the TileLink specification. Additional support features include separate address/control and data phases, and the ability to issue multiple outstanding transactions, out-of-order transaction completion, burst transfers, atomic operation and hint operation. A rich set of configuration parameters controls TileLink functionality.

SmartDV will demonstrate the TileLink VIP and other smart VIP solutions in booth #801 during DVCon Monday, February 25, through Wednesday, February 27, at the DoubleTree Hotel in San Jose, Calif.

Pricing and Availability

The SmartDV TileLink Verification IP is shipping now. Pricing is available upon request. To learn more, visit www.Smart-DV.com

About SmartDV

SmartDV™ Technologies, the ***Proven*** and ***Trusted*** choice for Verification IP, offers high-quality standard and custom protocol Verification IP supporting all simulation, emulation, formal verification tools and verification languages used in a coverage-driven chip design verification flow. Design groups worldwide rely on SmartDV's Verification IP solutions developed by talented and experienced ASIC and SoC design verification engineers for verification of their networking, storage, automotive, bus, MIPI and display chip projects. The result is Proven and Trusted Verification IP used in hundreds of projects throughout the global electronics industry. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif.

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