News Release

SmartDV™

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SmartDV Unveils SimXL Portfolio of Synthesizable Transactors for Hardware Emulation, FPGA Prototyping Platforms

Reusable Plug-and-Play Solution Enables Verification Engineers to Build System-Level SoC Test Environment

SAN JOSE, CALIF — February 14, 2019 — SmartDV™ Technologies, the ***Proven*** and ***Trusted*** choice for Verification IP, today unveiled SimXL™, its portfolio of Synthesizable Transactors for accelerating system-level, system-on-chip (SoC) testing on hardware emulators or field programmable gate array (FPGA) prototyping platforms.

SimXL, a configurable, reusable plug-and-play verification solution for interfaces based on industry-standard hardware verification languages (HVLs), runs on Cadence® Palladium®, Veloce® Strato™ from Mentor, a Siemens Business, Synopsys' ZeBu® and any custom FPGA prototyping tool.

It is fully compliant with most popular standards' specifications, including automotive, serial bus, memory, MIPI, networking, SoC interconnect fabrics, storage and video protocols.

Developed with the same functionality and performance as SmartDV's Verification IP for simulation, SimXL offers fast execution speed with advanced

commands, configurations and a status reporting interface for ease of use and debug. An interface based on UVM, OVM, SystemVerilog, SystemC controls SimXL.

Full API compatibility enables designs to move seamlessly from simulation to emulation. A synthesizable register transfer level (RTL) interface with a testbench written in C/C++, SystemC or SystemVerilog links to a design under test (DUT) mapped onto the emulator or FPGA prototyping tool to mimic a specific protocol. Virtual device models, application specific logs, consistency checkers, virtual speed adapters to real hardware and networks, data analysis and export functions provide the protocol-specific tools to evaluate test results.

“Our mission is to provide a full complement of high-quality, cost-effective Verification IP solutions along with superior support and service,” says Deepak Kumar Tala, chairman of SmartDV. “SimXL is an example of our commitment to this goal. It leverages the expertise of SmartDV’s ASIC and SoC design verification engineers, each of whom has a rich skillset of experience in HVLs and hardware emulation.”

SmartDV will demonstrate SimXL, and its smart VIP solutions in booth #801 during DVCon. DVCon will be held Monday, February 25, through Wednesday, February 27, at the DoubleTree Hotel in San Jose, Calif.

Pricing and Availability

The SmartDV portfolio of SimXL Verification IP is shipping now. A list of available SimXL VIP models is available at www.Smart-DV.com

Pricing is available upon request.

About SmartDV

SmartDV™ Technologies, the ***Proven*** and ***Trusted*** choice for Verification IP, offers high-quality standard and custom protocol Verification IP supporting all simulation, emulation, formal verification tools and verification languages used in a coverage-driven chip design verification flow. Design groups worldwide rely on SmartDV's Verification IP solutions developed by talented and experienced ASIC and SoC design verification engineers for verification of their networking, storage, automotive, bus, MIPI and display chip projects. The result is Proven and Trusted Verification IP used in hundreds of projects throughout the global electronics industry. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif.

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